IFW

Attorney's Docket No. 004363.P005C PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

David M. Colleran

Application No.: 10/810,444

Filed: March 26, 2004

For: Automatic Phase Lock Loop Design Using Geometric Programming

Examiner: Not Yet Assigned

Art Unit: Not Yet Assigned

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed for applications filed after June 30, 2003). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on 9-2-04.
(Date of Deposit)

Tina Wainright
(Typed or printed name of person mailing correspondence)

T. Wainright
(Signature of person mailing correspondence)

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

__X__ 37 C.F.R. §1.97(b).

_____ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

____ A statement pursuant to 37 C.F.R. §1.97(e) or

____ A check for $180.00 for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A statement pursuant to 37 C.F.R. §1.97(e); and

(2) A check for $180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 9/2, 2004

Chui-Kiu Teresa Wong
Reg. No. 48,042

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 720-8300

Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	10/810,444
Filing Date	March 26, 2004
First Named Inventor:	David M. Colleran
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	004363.P005C

Sheet	1	of	3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	6,578,179 B2	06-10-2003	Shirotori, et al.	
		US-	6,574,786 B1	06-03-2003	Pohlenz, et al.	
		US-	6,539,533 B1	03-25-2003	Brown, III et al.	
		US-	6,581,188	06-17-2003	Hosomi, et al.	
		US-	6,311,315	10-30-2001	Tamaki	
		US-	6,002,860	12-14-1999	Voinigescu, et al.	
		US-	5,754,826	05-19-1998	Gamal, et al.	
		US-	5,633,807	05-27-1997	Fishburn, et al.	
		US-	5,055,716	10-08-1991	El Gamel	
		US-	5,289,021	02-22-1994	El Gamel	
		US-				
		US-				
		US-				
		US-				
		US-				

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/810,444
				Filing Date	March 26, 2004
				First Named Inventor:	David M. Colleran
				Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	2	**of**	3	Attorney Docket Number	004363.P005C

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		HERSHENSON, M., et al., "GPCAD: A Tool for CMOS Op-Amp Synthesis" 8 pages, Proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 296-303, November 1998.	
		HERSHENSON, M., et al., "Posynomial models for MOSFETs" 9 pages, July 7, 1998.	
		CHANG, H, et al., "A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits" 6 pages, IEEE 1992 Custom Integrated Circuits Conference.	
		CHAVEZ, J., et al, "Analog Design Optimization: A Case Study" 3 pages, IEEE, January 1993.	
		GEILEN, G., et al., "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing", pp. 707-713, IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, June 1990.	
		FISHBURN, J, et al., "TILOS: A Posynomial Programming Approach to Transistor Sizing" pp. 326-328, IEEE, 1985.	
		MAULIK, P., et al., "Integer Programming Based on Topology Selection of Cell-Level Analog Circuits", 12 pages, IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 14, No. 4, April 1995.	
		SWINGS, K., et al., "An Intelligent Analog IC Design System Based On Manipulation Of Design Equations" pp. 8.6.1- 8.6.4, IEEE 1990, Custom Integrated Circuits Conference.	
		NESTEROV, Y., et al., "Interior-Point Polynomial algorithms in Convex Programming" 8 pgs., 1994, Society for Industrial and Applied mathematics.	
		YANG, H.Z., et al., "Simulated Annealing Algorithm with Multi-Molecule: an Approach to Analog Synthesis" pp. 571-575, IEEE, 1996.	
		WONG, D.F., et al., "Simulated Annealing For VLSI Design" 6 pages, 1998, Kulwer Academic Publishers.	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English Translation is attached.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/810,444
				Filing Date	March 26, 2004
				First Named Inventor:	David M. Colleran
				Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	3	**of**	3	Attorney Docket Number	004363.P005C

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		MAULIK, P., et al., "Sizing of Cell-Level Analog Circuits Using Constrained Optimization Techniques" pp. 233-241, IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993.	
		OCHOTTA, E, et al., "Synthesis of High –Performance Analog Circuits in ASTRX/OBLS" pp. 273-295, IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 15, No. 3, March 1996.	
		WRIGHT, S., "Primal-Dual Interior-Point Methods" pp. 1-3, http://www.siam.org/books/wright, Printed August 19, 1998.	
		SHYU, J., et al., "Optimization-Based Transistor Sizing" pp. 400-408, IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1998.	
		WRIGHT, S., "Primal-Dual Interior-Point Methods" 14 pages, 1997, Society for Industrial and Applied Mathematics.	
		VAN LAARHOVEN, P.J.M., et al., "Simulated Annealing: Theory and Applications" 26 pages, 1987, Kulwer Academic Publishers.	
		HERSHENSON, M., et al., "CMOS Operational Amplifier Design and Optimization via Geometric Programming" pp. 1-4, Analog Integrated Circuits, Stanford University.	
		AGUIRRE, M.A., et al., "Analog Design Optimization by means of a Tabu Search Approach" pp. 375-378.	
		MEDEIRO, F., et al., "A Statistical Optimization-Based Approach for Automated Sizing of Analog Cells", pp. 594-597, Dept. of Analog Circuit Design.	
		SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering.	
		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.	
		VASSILIOU, I., et al, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology" 6 pages.	
		SAPATNEKAR, S, et al., "An Exact Solution to the Transistor Sizing Problem for CMOS Circuits Using Convex Optimization" 35 pages.	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English Translation is attached.